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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,488	09/29/2000	Lester J. Kozlowski	24096.00700	1319

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EXAMINER	
EDWARDS, PATRICK L	
ART UNIT	**PAPER NUMBER**
2621	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,488	KOZLOWSKI, LESTER J.	
	Examiner	Art Unit	
	Patrick L Edwards	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10,12,14-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-21* is/are allowed.

6)☒ Claim(s) *1,4-10,12,14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15 September 2005 has been entered.

Response to Arguments

2. The applicant's arguments, filed on 15 September 2005, have been fully considered. A response to these arguments is provided below.

Drawing Objections

Summary of Argument: Applicant has submitted corrected drawings, and notes that these drawings correct a previous drafting error. Specifically, transistor M102 was initially shown (in the previous drawings) as having a source connected to ground. The corrected drawings show that M102 should be connected to a node between M105 and Vdrain.

Examiner's Response: The examiner agrees that no new matter has been added by this drawing correction, and has no problem with the contents of the drawing correction. However, the applicant is required to submit formal replacement sheets in compliance with 37 C.F.R. § 1.121(d). Further, the drawing changes do not comply with 37 C.F.R. § 1.84(l) because the newly added hand-written lines are not uniformly thick and well-defined. New corrected drawings are required in reply to the office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Prior Art Rejections

Summary of Argument: Applicant traverses the claim rejections under 35 U.S.C § 103(a) set forth in the the final rejection mailed on 05-17-2004. Although applicant admits that the rejection meets all of the claimed limitations, applicant argues that "This is an insufficient basis to prove that the specific combination of elements as disclosed in the present application would have been obvious to one of skill in the art" (see 'remarks' pg. 7, bottom paragraph).

Applicant further argues that the examiner has not considered how the specific references teach away from the present invention, and that it is not clear that any of the hypothetical combinations proposed by the examiner would even function (see 'remarks' pg. 8).

Examiner's Response: Applicant's arguments are not persuasive. In response to the first argument, the previous action expressly provided a motivation to combine references. This motivation is sufficient.

In response to the second argument, applicant is reminded that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-7, 10, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1), and Kozlowski et al. (U.S. Patent No. 6,493,030 B1).

With respect to claim 1, Fossum discloses an active pixel sensor circuit comprising: a photodetector (see Fig. 2A: Reference numeral 200).

Fossum further discloses a reset transistor connected between the photodetector and a first bus (see Fig. 2A: Reference numeral 204, referring to transistor M1, which is connected between the photodiode 200 and VDR (i.e. a first bus).).

Fossum further discloses a snapshot transistor having a node connected to the photodetector (see Fig. 2A: Reference numeral 210, referring to transistor M2, which has a node connected to the photodiode 200.)

Fossum further discloses a driver transistor connected to the snapshot transistor (see Fig. 2A: Reference numeral 216, referring to transistor M4, which is connected to transistor M2 (i.e. the snapshot transistor).). Figure 2A of Fossum further shows that the driver transistor M4 (reference numeral 216) is connected to transistor M5 (reference numeral 224). The gate of transistor M5 is a row driver bus (see fig. 2A in conjunction with the first two lines of paragraph [0043]). Thus, the driver transistor M4 is to a row driver bus and the snapshot transistor as required by the claim.

Fossum further discloses an isolation transistor connected between the driver transistor and a column bus (see Fig. 2A: Reference numeral 224, referring to transistor M5, which is connected between transistor M4 (i.e. the driver transistor) and column output bus 226.).

Fossum further discloses that the transistors are MOSFETs (see paragraph [0022]: The reference describes that transistors are FETs.).

While Fossum also discloses the use of a reset signal, RPD, to reset the photodiode, the reference does not disclose that the reset signal is a tapered signal. Kozlowski et al., in the same field of endeavor of active pixel sensors, and the same problem solving area of reset signals, discloses the use of a tapered reset signal (see Fig. 9).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Fossum by adding the tapered reset signal as taught by Kozlowski et al. because the use of a tapered reset waveform allows for "a row [to be] resettable to within tens of microseconds for full noise suppression" (see Kozlowski et al.: column 6, lines 51-53). Therefore, the photodiodes of the system can be reset quickly while also suppressing any noise in the signal.

With respect to claim 4, Fossum discloses that a charge from the photodiode is transferred to a gate capacitance of the driver transistor via the snapshot transistor (see paragraph [0031]: The reference describes that the photosignal (i.e. charge) collected by the photodiode trickles over the TX barrier, which is part of transistor M2 (i.e. a snapshot transistor), to node FD, which is equivalent to the gate capacitance of transistor M4 (i.e. the driver transistor).).

With respect to claim 5, Fossum discloses that the reset transistor discharges any charge left on the photodetector along with any charge on the gate of the driver transistor during a reset operation (see paragraph [0030]: The reference describes that the initial state of the photodiode is erased by the reset operation performed by transistor M1 (i.e. discharges any charge left on the photodetector along with any charge on the gate of the driver transistor during a reset operation).).

With respect to claim 6, Fossum discloses that the reset transistor is disabled during a signal integration mode and a snapshot image capture mode (see Fig. 3C and paragraph [0031]: The reference describes that after the reset, the signal integration and image capture mode are executed. Furthermore, as can be seen in Fig. 3C, no signal is produced for RFD which disables transistor M1 (i.e. the reset transistor).).

With respect to claim 7, Fossum discloses that, after snapshot image capture, the reset transistor is enabled in order to drain any unwanted charge that is generated after the integration mode (see paragraph [0033]: The reference discloses that after the image has been captured, transistor M1 (i.e. the reset transistor) drains all additional photoelectrons form PD down to the level of RFD.).

With respect to claim 10, all of the limitations of the claim have been addressed in the claim 1 discussion above. The only difference between the claims is that claim 10 requires an "amplifier means for amplifying the signal from the snapshot means." The Fossum reference discloses this limitation (see Fig. 2A and paragraph [0024]: The reference describes that transistor 216 acts as an amplifier.).

With respect to claim 14, all of the limitations of the claim have been addressed in the claim 1 discussion above.

With respect to claim 15, Fossum discloses that the reset, snapshot, driver and isolation MOSFETs are all of the same polarity (see Fig. 2A and paragraph [0023]: The reference describes that transistor 210 is an n-well implementation. As can be seen in Fig. 2A, all of the transistors in the schematic are represented by the same symbol. Therefore, all of the transistors have an n-well implementation and are of the same polarity.).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1) and Kozlowski et al. (U.S. Patent No. 6,493,030 B1), With respect to claim 7 above, and further in combination with Uno (U.S. Patent No. 5,296,696 A).

Claim 8 calls for a column buffer to be connected to the column bus. A column buffer is not disclosed by the combination of Fossum and Kozlowski et al. However, Uno, in the same field of endeavor of solid-state image pickup devices discloses the use of such a column buffer (see Fig, 5 and column 4, lines 65-68: The reference describes that an FPN suppression circuit (i.e. a column buffer) is inserted between the column bus and the pixel circuit.).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Fossum and Kozlowski et al. by adding the column buffer as taught in Uno because such a device because such a device suppressed fixed pattern noise while enabling "large output gain and non-destructive readout even with large parasitic capacitances of signal lines" (see Uno: column 3, lines 29-31).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1), Kozlowski et al. (U.S. Patent No. 6,493,030 B1), and Uno (U.S. Patent No. 5,296,696 A), With respect to claim 8 above, and further in combination with Barna et al. (U.S. Patent No. 6,445,022 B1).

Claim 9 calls for a row driver connected to the driver transistor. A row driver is absent from the combination of Fossum, Kozlowski et al., and Uno; however, such a component is disclosed in Barna et al. (see Fig. 5: Reference numeral 508 referring to Row Drivers).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Fossum, Kozlowski et al., and Uno by adding a row driver as disclosed by Barna et al. because the use of a row driver allows the "image array [to be] read out a row at a time" (see Barna et al.: column 3, lines 63-64).

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1) and Kozlowski et al. (U.S. Patent No. 6,493,030 B1), With respect to claim 15 above, and further in combination with Barna et al. (U.S. Patent No. 6,445,022 B1).

Claim 16 calls for a row driver circuit. A row driver circuit is absent from the combination of Fossum and Kozlowski et al.; however Barna et al. discloses the use of such a circuit as described in the rejection of claim 9 above.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Fossum and Kozlowski et al. by adding the row driver circuit disclosed by Barna et al. for the same reasons as described above in the rejection of claim 9.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1), Kozlowski et al. (U.S. Patent No. 6,493,030 B1), and Barna et al. (U.S. Patent No. 6,445,022 B1), With respect to claim 16 above, and further in combination with Uno (U.S. Patent No. 5,296,696 A).

Claim 17 calls for a column buffer circuit to be connected to the column bus. A column buffer is not disclosed by the combination of Fossum, Kozlowski et al., and Barna et al. However, Uno, in the same field of endeavor of solid-state image pickup devices discloses the use of such a column buffer as described above in the rejection of claim 8.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Fossum, Kozlowski et al., and Barna et al. by adding the column buffer taught in Uno for the same reasons as described above in the rejection of claim 8.

Allowable Subject Matter

9. Claims 19-21 are allowed.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Fossum et al. (USPN 5,841,126) teaches a CMOS active pixel sensor type imaging system
- Fossum (USPN 6,005,619) teaches efficiency improvements in active pixel sensors
- Fossum et al. (USPN 6,166,768) teaches an active pixel sensor array with simple floating gate pixels.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick L Edwards whose telephone number is (703) 305-6301. The examiner can normally be reached on 8:30am - 5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (703)308-5246. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patrick L Edwards

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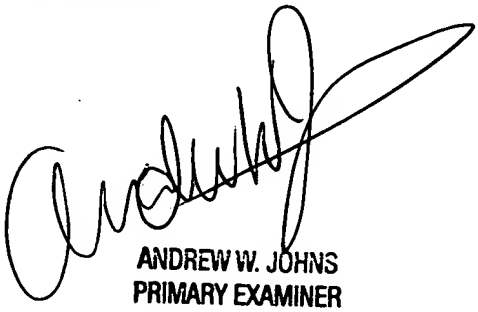
Art Unit 2621



ANDREW W. JOHNS
PRIMARY EXAMINER